IN THE SPECIFICATION:

Please replace paragraph number **[0002]** with the following rewritten paragraph:

[0002] State of the Art: Electrostatic discharge (hereinafter "ESD") and electrical overstress (hereinafter "EOS") are two common phenomenon that occur during human or mechanical handling of semiconductor integrated circuitry (hereinafter "IC") devices. The input pins to an IC device are highly sensitive to damage from the voltage spike of an ESD, which can reach potentials in excess of hundreds of volts. If a charge of this magnitude is brought into contact with a pin of an IC device, a large flow of current may surge through the IC device. Although this current surge may be of limited energy and duration, it can cause a breakdown of insulating barriers within the IC device (usually gate oxide insulating barriers of an MOS ~~(metal-oxide-semiconductor)~~ (metal-oxide-semiconductor) IC device). This breakdown of the insulating barriers within an IC device can result in permanent damage to the IC device and, once damaged, it is impossible to repair the IC device.

Please replace paragraph number **[0058]** with the following rewritten paragraph:

[0058] A third barrier layer 166 (preferably made of borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), or the like) is deposited over the second barrier layer 128 and the contact lands 158, and, optionally, planarized, as shown in FIG. 17. A second etch mask 168, such as photoresist, is deposited on the third barrier layer 166, wherein the second etch mask 168 includes openings 172 substantially aligned over the contact lands 158, as shown in FIG. 18. The third barrier layer 166 is then etched down to the contact lands 158 to form contact vias 174, as shown in FIG. 19, and the second etch mask 168 is then removed, as shown in FIG. 20.